anticipated by Zenke (U.S. Patent No. 5,811,333); and rejected claim 15 under 35 U.S.C. § 103(a) as unpatentable over Zenke in view of Kashihara.

Regarding the claims, Applicants respectfully traverse the rejection of claims 10, 14, 15, 19, and 24, as detailed above, for the following reasons.

Regarding the Examiner's objection to claims 10 and 19 in item 2 of the Office Action for "informalities," Applicants submit that the amendments to claims 10 and 19 have sufficiently addressed the Examiner's objection. Applicants therefore deem the objection to claims 10 and 19 overcome.

In order to establish that Kashihara or Zenke anticipates Applicants' claimed invention under 35 U.S.C. § 102, each and every element of the claim in issue must be found, either expressly described or under principles of inherency, in a single prior art reference. Furthermore, the single prior art reference must disclose all of the claimed elements "in as complete detail as is contained in the ... claim." See M.P.E.P. § 2131, 8th Ed., Aug. 2001, p.2100-69, quoting *Richardson v. Suzuki Motor Co.*, 9 U.S.P.Q.2d 1913, 1920 (Fed. Cir. 1989).

Regarding the 35 U.S.C. § 102(b) rejection of claim 19, Kashihara does not teach each and every element of Applicants' present invention as claimed. Applicants' claim 19 recites, *inter alia*, "a lower electrode formed in contact with the conductive plug and having a side and upper surface, a surface area of the side being larger than a surface area of the upper surface," and "a capacitor insulating film formed on a side of the lower electrode; and an upper electrode formed above the lower electrode via the capacitor insulating film, the capacitor insulating film being formed above a top surface of the lower electrode via a second insulating film different from the capacitor insulating film."

In contrast, Kashihara teaches a lower electrode layer 1 formed in contact with a barrier metal layer 13 on plug layer 43a. See Kashihara's Figure 1. Kashihara does not disclose anything about the lower electrode having a side and upper surface, ***a surface area of the side***

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being larger than a surface area of the upper surface. Further, Kashihara teaches a capacitor insulating layer 3 formed on lower electrode layer 1. Kashihara does not disclose anything about the capacitor insulating layer 3 being formed above a top surface of the lower electrode layer 1 via a ***second insulating film different from the capacitor insulating film***. Thus, Kashihara does not disclose each and every element of Applicants' claim 19.

Since Kashihara does not disclose each and every element of Applicants' claim 19, Kashihara cannot anticipate Applicants' claim 19. Therefore, Applicants respectfully submit that claim 19 is patentable over Kashihara, and submit that the Examiner should withdraw the 35 U.S.C. § 102(b) rejection.

Regarding the 35 U.S.C. § 102(b) rejection of claims 10, 14, 19, and 24, Zenke does not teach each and every element of Applicants' present invention as claimed. Applicants' claim 10 recites, *inter alia*, "a conductive plug formed on the semiconductor substrate; a lower electrode formed in contact with the conductive plug and constituted by a plurality of crystal grains, the crystal grains containing a metallic element; a capacitor insulating film formed on a side of the capacitor lower electrode; and an upper electrode formed above the lower electrode via the capacitor dielectric film, a grain boundary between adjacent two of said plurality of crystal grains constituting the lower electrode being substantially perpendicular to an interface between the lower electrode and the capacitor insulating film."

Zenke instead discloses a Si-oxide layer 2 in which contact hole 2a is formed; then first poly-Si layer 3 is formed on Si-oxide layer 2 and in contact hole 2a. Poly-Si layer 3 becomes lower electrode 4, on which capacitor insulating layer 5 and second poly-Si layer 6 are formed. Second poly-Si layer 6 is formed into upper electrode 7. See Zenke's Figures 3A – 3D. Zenke discloses nothing about a conductive plug formed on the semiconductor substrate, since lower electrode 4 is formed contiguously on capacitor insulating layer 5 and in contact hole 2a. Applicants disagree with the Examiner's statements in item 4, page 3 of the Office Action, which

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describes Zenke's first poly-Si layer 3 as being split into a conductive plug and lower electrode. Zenke does not disclose at least "a lower electrode formed in contact with the conductive plug" (Applicants' claim 10) and teaches nothing about the first poly-Si layer (lower electrode) ***having*** "***crystal grains containing a metallic element***" (Applicants' claim 10, emphasis added). Zenke's poly-Si lower electrode 4, by its nature, does not contain a metallic element. Furthermore, Zenke does not teach anything about "an upper electrode formed above the lower electrode via the ***capacitor dielectric film***" (Applicants' claim 10, emphasis added), since Zenke only teaches "a thin silicon nitride layer and a silicon oxide layer are successively deposited ... to form a ***capacitor insulator layer*** 5" (Zenke, column 6, lines 12 – 15, emphasis added).

Finally, Zenke does not disclose that the grain structure of the poly-Si layer contains grains wherein "a grain boundary between adjacent two of said plurality of crystal grains constituting the lower electrode being substantially perpendicular to an interface between the lower electrode and the capacitor insulating film" (Applicants' claim 10). In fact, Zenke teaches ***away*** from this feature: "the lower electrode 4 has the roughened surface 3*a* formed by etching the first polysilicon layer 3 of a random crystal structure. In the random crystal structure, the grains and grain boundaries are distributed at random both at top and side surfaces of the lower electrode 4" (Zenke, column 6, lines 22 – 27). Thus, Zenke does not disclose each and every element of Applicants' claim 10.

Likewise, Zenke does not disclose each and every element of Applicants' claim 19, which recites, *inter alia*, "a conductive plug formed on the semiconductor substrate; a lower electrode formed in contact with the conductive plug and having a side and upper surface, a surface area of the side being larger than a surface area of the upper surface; a capacitor insulating film formed on a side of the lower electrode" and "the capacitor insulating film being formed above a top surface of the lower electrode via a second insulating film different from the capacitor insulating film."

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As argued above regarding recitations in Applicants' claim 10, Zenke, likewise, does not disclose at least the abovementioned recitations of Applicants' claim 19. In particular, Zenke does not teach anything about the surface area of lower electrode 4, which, as depicted in Zenke's Figure 3D, has a larger surface area on the upper surface. Furthermore, Zenke only discloses capacitor insulator layer 5, and not a "capacitor insulating film being formed above a top surface of the lower electrode ***via a second insulating film different from the capacitor insulating film***." (Applicants' claim 19, emphasis added). Thus, Zenke does not disclose each and every element of Applicants' claim 19.

Since Zenke does not disclose each and every element of Applicants' claims 10 and 19, Zenke does not anticipate Applicants' claims 10 and 19. Therefore, Applicants respectfully submit that claims 10 and 19 are patentable over Zenke, as are claims 14 and 24, at least by virtue of their dependence from allowable base claim 10. Applicants submit that the Examiner should withdraw the 35 U.S.C. § 102(b) rejection.

Regarding the 35 U.S.C. § 103(a) rejection of claim 15, Applicants respectfully disagree with the Examiner's arguments and conclusions. "To establish *prima facie* obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. ... If an independent claim is nonobvious under 35 U.S.C. § 103, then any claim depending therefrom is nonobvious." See M.P.E.P. § 2143.03, 8th Ed., Aug. 2001, p. 2100-26.

Applicants have already demonstrated that Zenke and Kashihara, taken alone or in combination, fail to suggest all of the features of independent claims 10 and 19, as argued above regarding the rejections made under 35 U.S.C. § 102(b). The Examiner has therefore not met one of the basic criteria for establishing a *prima facie* case of obviousness, wherein "the prior art reference (or references when combined) must teach or suggest all the claim limitations." See M.P.E.P. §§ 2142, 2143, and 2143.03. Thus, since independent claim 10 is deemed allowable as already argued, dependent claim 15 is also allowable at least by virtue of its dependence from

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base claim 10. Therefore Applicants respectfully submit that the Examiner should withdraw the 35 U.S.C. § 103(a) rejection.

At least for the abovementioned reasons, Applicants respectfully submit that independent claims 10 and 19 should be allowed, as should claims 14, 15, and 24, at least by virtue of their dependence from allowable base claim 10.

In view of the foregoing, Applicants respectfully request that the Examiner withdraw the rejection of claims 10, 14, 15, 19, and 24 under 35 U.S.C. § 102(b) and 35 U.S.C. § 103(a), as detailed at the beginning of this Amendment. A favorable action is requested.

If any extension of time is required under 37 C.F.R. § 1.136 to obtain entry of this response, and not requested by attachment, such extension is hereby requested. If there are any fees due under 37 C.F.R. § 1.16 or 1.17 that are not authorized including any fees required for an extension of time under 37 C.F.R. § 1.136, please charge those fees to our Deposit Account No. 06-0916.

Respectfully submitted,

FINNEGAN, HENDERSON, FARABOW,
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Dated: January 14, 2002

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APPENDIX TO AMENDMENT OF January 14, 2002

Version of Claims with Markings to Show Changes Made

AMENDMENTS TO THE CLAIMS:

Please amend claims 10 and 19 as follows:

10. (Amended) A semiconductor device comprising:

a semiconductor substrate;

a conductive plug formed on the semiconductor substrate;

a lower electrode formed in contact with the conductive plug and constituted by a plurality of crystal grains, the crystal grains containing a metallic element;

a capacitor insulating film formed on a side of the capacitor lower electrode; and

[a] an upper electrode formed above the lower electrode via the capacitor dielectric film,

a grain boundary between adjacent two of said plurality of crystal grains constituting the lower electrode being substantially perpendicular to an interface between the lower electrode and the capacitor insulating film.

19. (Amended) A semiconductor device comprising:

a semiconductor substrate;

a conductive plug formed on the semiconductor substrate;

a lower electrode formed in contact with the conductive plug and having a side and upper surface, a surface area of the side being larger than a surface area of the upper surface;

a capacitor insulating film formed on a side of the lower electrode; and

[a] an upper electrode formed above the lower electrode via the capacitor insulating film,

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the capacitor insulating film being formed above a top surface of the lower electrode via a second insulating film different from the capacitor insulating film.

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